

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

**Methods of Forming Silicon-Doped Aluminum
Oxide, and Methods of Forming Transistors and
Memory Devices**

* * * * *

INVENTORS

Kie Y. Ahn
Leonard Forbes

EL 465852856

ATTORNEY'S DOCKET NO. MI22-1533

1 Methods of Forming Silicon-Doped Aluminum Oxide, and Methods
2 of Forming Transistors And Memory Devices

3 TECHNICAL FIELD

4 The invention pertains to methods of forming silicon-doped
5 aluminum oxide, and in particular embodiments pertains to methods of
6 forming transistor structures and memory devices.

7
8 BACKGROUND OF THE INVENTION

9 As silicon device sizes become increasingly smaller, it can be
10 increasingly difficult to form gate insulators capable of maintaining the
11 capacitance of a dynamic random access memory (DRAM) cell in the
12 range of 30 femptofarads (fF). Such capacitance is desired to achieve
13 immunity to radiation and soft errors, and to keep noise to acceptable
14 levels.

15 A commonly utilized dielectric material is silicon dioxide (SiO_2).
16 However such can be difficult to utilize in the 30 fF regime because the
17 dielectric becomes so thin that direct band-to-band tunneling current or
18 Fowler-Nordheim tunneling current becomes problematic. Accordingly,
19 there has been an effort to utilize high-k (i.e., high dielectric constant)
20 films (such as Al_2O_3 , Ta_2O_5 , and TiO_2), as materials to substitute for the
21 very thin silicon dioxide as dielectric materials in semiconductor devices.

22 Of the listed high-k materials, aluminum oxide has received
23 significant interest. Aluminum oxide has been used as a high-k inter-

poly dielectric (IPD) for low voltage/high speed flash memories. Specifically, it has been shown that 10 nanometer thick Al_2O_3 , with k of about 10, can reduce an erasing time by three orders of magnitude in comparison with 15 nanometer thick ONO (with ONO referring to a sandwich of silicon dioxide, silicon nitride, and silicon dioxide). The ONO has a k of about 10. Aluminum oxide can reduce the erasing of voltage a flash memory device by about 40% compared with silicon dioxide, and about 27% compared with ONO of the same thickness as the aluminum oxide.

Difficulties associated with Al_2O_3 films include that the optical properties of the films can vary significantly depending on the substrate that the film is grown on. For instance, studies have been done in which Al_2O_3 films have been grown by atomic layer deposition on Si, SiO_2 and TiN, and the studies have found significant differences in the optical properties of the film depending on the underlying substrate.

There has recently been some investigation on the effects of dopant addition to aluminum oxide which indicates that particular dopants can improve the properties of aluminum oxide. Specifically, the studies indicate that either silicon or zirconium can be added to an aluminum material to form a doped Al_2O_3 film with low leakage current and high thermal stability (up to 800°C), and with a dielectric constant greater than 8. It can be preferred to keep the dielectric constant high, and preferably to keep the dielectric constant above 10, as there is likely

1 a limited opportunity for dielectric materials with a constant less than
2 10 to replace silicon dioxide. However, alternate gate dielectrics having
3 dielectric constants greater than 10, and more preferably greater than 15,
4 may ultimately be desired as replacements for the silicon dioxide
5 materials currently being utilized.

6 Some work with aluminum oxide has focused on methods of
7 deposition of thin films of aluminum oxide. For instance, there has
8 been development of procedures for atomic layer deposition (ALD) of
9 aluminum oxide to DRAM and FeRAM (ferroelectric random access
10 memory). It is found that ALD films typically have lower leakage
11 current and larger dielectric breakdown voltage than conventional thermal
12 oxide materials. The leakage characteristics of MIS aluminum oxide
13 capacitors are lower than that of MIS-Ta₂O₅ capacitors. Also, it is
14 found that the ALD aluminum oxide can have low leakage and low
15 interface surface state densities.

16 A method of forming thin aluminum oxide films is to evaporate
17 sapphire (a form of high-purity aluminum oxide), and to subsequently
18 condense the evaporated material on a substrate. Sapphire can be
19 evaporated by, for example, electron gun evaporation or ion beam
20 evaporation (also called ion beam deposition). It is noted that aluminum
21 oxide films have also been deposited by thermal evaporation of single
22 crystal sapphire. In some instances, aluminum oxide can be evaporated
23 and deposited within a vacuum chamber under conditions in which no

1 additional oxygen is admitted to the vacuum chamber during evaporation,
2 and in which a substrate temperature is varied between 80°C and 140°C.
3 A typical deposition rate can be from about 10Å per second to about
4 12Å per second. The electrical breakdown voltage and resistivity can be
5 improved at higher substrate temperatures. It is found that if the films
6 are exposed to 98% relative humidity, the breakdown voltage can change
7 to a significantly lower value, such as, for example, to a value of from
8 about 10⁶ volts/cm to about 10⁴ volts/cm.

9 The aging properties of electron gun evaporated alumina films have
10 been investigated by mass spectrometry and IR spectrometry. It has
11 been found that if films are stored under normal atmospheric conditions,
12 a characteristic absorption's peak will appear in the infrared reflection
13 spectra which has been attributed to a build-up of water in the Al₂O₃
14 films. Such can cause the films to lose dielectric properties, and the
15 breakdown voltage can decrease by several orders of magnitude.

16 Subsequent studies using electron-optical examination of the cross-
17 section of vacuum-deposited aluminum oxide films shows that the films
18 are amorphous on cold substrates. However, as the substrate
19 temperature increases, an acicular crystalline structure appears for films
20 having thicknesses on the order of 100 nanometers, with typical column
21 diameters of from about 12 nanometers to about 17 nanometers. Such
22 structure leads to high film porosity, with a considerable fraction of the
23 pores extending through the entire thickness of the structure and being

filled with water if a humidity is 70% and higher. Other reports have described a porosity of about 5% for films prepared at 60°C. The relative porosity of aluminum oxide is also evidenced by examination of the protective properties of aluminum oxide layers (100 nanometers) prepared at room temperature on silver mirrors. Specifically, the films are found to not exhibit protective properties against corrosive agents such as water and hydrogen sulfide.

Studies of electron-beam evaporated aluminum oxide films grown under oxygen ion bombardment indicate that an index of refraction, and accordingly the film density, first rises, and then decreases with increasing ion current density for substrate temperatures between 70°C and 250°C. Ion bombardment during deposition is thought to cause the film to become more compact by inhibiting columnar growth.

Similar investigations on the effect of plasma activation on the phase transformation of aluminum oxide films have been done with films deposited by reactive high-rate electron beam evaporation. Plasma activation of the vapor took place via a hollow-cathode plasma. Aluminum oxide films deposited at 500°C and 700°C without plasma activation were characterized by columnar structure, and exhibited a relatively high porosity. However, films deposited with plasma activation at the same temperatures showed glassy fracture and a much denser microstructure.

1 It would be desirable to develop improved methods for forming
2 aluminum oxide films suitable for utilization as dielectric materials in
3 semiconductor structures, such as, for example, aluminum oxide films
4 suitable as dielectric materials in transistor gate structures and flash
5 memory device structures.

6 7 SUMMARY OF THE INVENTION

8 In one aspect, the invention encompasses a method of forming a
9 silicon-doped aluminum oxide. Aluminum oxide and silicon monoxide are
10 co-evaporated. Subsequently, at least some of the evaporated aluminum
11 oxide and silicon monoxide is deposited on a substrate to form the
12 silicon-doped aluminum oxide on the substrate.

13 In another aspect, the invention encompasses a method of forming
14 a transistor. An insulating layer of silicon-doped aluminum oxide is
15 formed over a substrate. The forming of the insulating layer of silicon-
16 doped aluminum oxide comprises co-evaporation of aluminum oxide and
17 silicon monoxide, and deposition of at least some of the evaporated
18 aluminum oxide and silicon monoxide on the substrate to form the
19 silicon-doped aluminum oxide on the substrate. A patterned conductive
20 material is formed over the insulating layer of silicon-doped aluminum
21 oxide. A pair of conductive source/drain regions are spaced from one
22 another by the patterned conductive material, with the conductive
23 material thus defining a transistor gate between the source/drain regions.

1 In yet another aspect, the invention pertains to methods of forming
2 flash memory devices.

3 4 **BRIEF DESCRIPTION OF THE DRAWINGS**

5 Preferred embodiments of the invention are described below with
6 reference to the following accompanying drawings.

7 Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor
8 substrate wafer fragment at a preliminary step of a method of the
9 present invention.

10 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a
11 processing step subsequent to that of Fig. 1.

12 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a
13 processing step subsequent to that of Fig. 2.

14 Fig. 4 is a view of the Fig. 1 wafer fragment shown at a
15 processing step subsequent to that of Fig. 3.

16 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a
17 processing step subsequent to that of Fig. 4.

18 Fig. 6 is a view of the Fig. 1 wafer fragment shown at a
19 processing step subsequent to that of Fig. 3 in one aspect of the
20 invention, and subsequent to that of Fig. 4 in another aspect of the
21 invention.

22 Fig. 7 is a view of the Fig. 1 wafer fragment shown at a
23 processing step subsequent to that of Fig. 6.

1 Fig. 8 is a diagrammatic, cross-sectional view of a semiconductor
2 substrate wafer fragment illustrating a flash memory device formed in
3 accordance with a method of the present invention.

4 Fig. 9 is a diagrammatic, cross-sectional view of a reaction chamber
5 illustrating a deposition process which can be utilized in methodology of
6 the present invention.

7 8 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

9 This disclosure of the invention is submitted in furtherance of the
10 constitutional purposes of the U.S. Patent Laws "to promote the progress
11 of science and useful arts" (Article 1, Section 8).

12 The invention encompasses an improved method of depositing
13 silicon-doped aluminum oxide films which can have high reliability
14 (specifically, for example, low leakage current and high thermal stability).
15 The films can be deposited by co-evaporation of aluminum-oxide and
16 silicon monoxide (SiO), and subsequent condensation of the co-evaporated
17 materials onto a substrate. More specifically, porous Al_2O_3 films can be
18 formed by electron gun-evaporation or ion beam deposition (in
19 accordance with the present invention, the evaporation of aluminum oxide
20 is conducted in high vacuum, and not in a partial pressure of oxygen).
21 Simultaneously with the formation of the porous aluminum oxide film,
22 silicon monoxide is thermally evaporated to produce a silicon dopant
23 which is incorporated into the aluminum oxide film during formation of

1 the film (i.e., *in situ* as the film forms). Any oxygen deficiency of the
2 evaporated aluminum oxide can be supplied by oxygen in the silicon
3 monoxide while the silicon of the silicon monoxide becomes a dopant
4 within the aluminum oxide film.

5 A relative concentration of silicon within the aluminum oxide can
6 be adjusted by controlling the evaporation rate of the silicon monoxide
7 relative to that of the aluminum oxide. Preferably, the films will have
8 at least 0.1 weight percent of silicon dopant provided within the
9 aluminum oxide, to a maximum of 30 weight percent of the silicon
10 dopant within the aluminum oxide. The films formed by methodology
11 of the present invention can be utilized as gate dielectric for various
12 semiconductor devices, such as, for example, MOS devices and flash
13 memory devices.

14 Methodology of the present invention is described with reference
15 to Figs. 1-9. Referring first to Fig. 1, a semiconductor wafer
16 fragment 10 is illustrated at a preliminary step of a method of the
17 present invention. Wafer fragment 10 comprises a substrate 12.
18 Substrate 12 can comprise, for example, monocrystalline silicon lightly-
19 background doped with a p-type dopant. To aid in interpretation of the
20 claims that follow, the terms "semiconductive substrate" and
21 "semiconductor substrate" are defined to mean any construction
22 comprising semiconductive material, including, but not limited to, bulk
23 semiconductive materials such as a semiconductive wafer (either alone or

1 in assemblies comprising other materials thereon), and semiconductive
2 material layers (either alone or in assemblies comprising other materials).
3 The term "substrate" refers to any supporting structure, including, but
4 not limited to, the semiconductive substrates described above.

5 Referring next to Fig. 2, wafer fragment 10 is shown at a
6 processing step subsequent to that of Fig. 1. Specifically, wafer fragment
7 10 is shown with an insulating dielectric layer 14 formed over
8 substrate 12. Dielectric layer 14 can comprise, for example, silicon-doped
9 aluminum oxide ($\text{Si-Al}_2\text{O}_3$).

10 Dielectric layer 14 can be formed by co-evaporation of aluminum
11 oxide and silicon monoxide, and subsequent condensation of the co-
12 evaporated materials onto substrate 12. An exemplary method of co-
13 evaporating and condensing aluminum oxide and silicon monoxide is
14 described with reference to Fig. 9, which shows a reaction chamber 100.
15 A vacuum can be provided within chamber 100, and O_2 can be precluded
16 from flowing into chamber 100. An aluminum oxide source 102 is
17 provided within chamber 100, and a silicon monoxide source 104 is also
18 provided within chamber 100. Aluminum oxide source 102 can comprise,
19 for example, single crystal sapphire.

20 A substrate 106 (which can comprise, for example, the wafer
21 fragment 10 of Fig. 2), is also provided within chamber 100, and is
22 shown on a substrate holder 108. Holder 108 can be provided with a
23 thermal control mechanism, such as, for example, a heater, or a cooler.

1 Holder 108 can thus be utilized to control a temperature of
2 substrate 106.

3 In operation, silicon monoxide is evaporated from source 104
4 (illustrated by arrow 110), and aluminum oxide is evaporated from 102
5 (illustrated by arrow 112) to form a vapor mixture of aluminum oxide
6 and silicon monoxide within chamber 100. The co-evaporated aluminum
7 oxide and silicon monoxide are co-condensed onto substrate 106 to
8 deposit dielectric layer 14 (not shown in Fig. 9) onto the substrate.

9 It is noted that chamber 100 is shown diagrammatically in Fig. 9,
10 and that numerous configurations of a reaction chamber can be utilized
11 in methodology of the present invention. Also, it is noted that even
12 though aluminum oxide and silicon monoxide are shown being co-
13 evaporated within reaction chamber 100, the invention encompasses other
14 embodiments (not shown) wherein one or both of the evaporated
15 aluminum oxide and silicon monoxide are formed outside of chamber 100
16 and subsequently flowed into chamber 100 to condense on substrate 106
17 and thereby deposit dielectric layer 14 onto the substrate.

18 The evaporation of silicon monoxide can be readily accomplished.
19 Silicon monoxide can be evaporated from a thermal source and deposited
20 onto a "cold" (room temperature) substrate with good adhesion. Silicon
21 monoxide films formed by thermal evaporation have many attractive
22 optical, electrical, mechanical and thermal properties, which can make it
23 suitable for many semiconductor applications. For instance, silicon

1 monoxide can be thermally evaporated at much lower temperatures than
2 silicon, silicon dioxide, or silicon nitride (Si_3N_4), and it condenses on
3 cooler substrates in a uniform and adherent stoichiometric silicon
4 monoxide film when evaporated at high vacuum. In fact, before the
5 present day technology of silicon dioxide deposition by CVD (chemical
6 vapor deposition), and when sputtering was not available, silicon
7 monoxide was deposited by thermal evaporation and subsequently oxidized
8 for rapid thermal oxidation. Such technique demonstrated the possibility
9 of converting silicon monoxide deposited at room temperature to silicon
10 dioxide by rapid thermal annealing at 700°C to $1,100^\circ\text{C}$, but with a
11 duration of only a few seconds, as compared with the ordinary thermal
12 oxidation which takes a period ranging from 30 to 60 minutes
13 at $1,000^\circ\text{C}$.

14 Another aspect of silicon monoxide chemistry is that it has been
15 shown that the production of silicon dioxide films on a large substrate
16 area by ion deposition of silicon monoxide can be accomplished. For
17 instance, silicon dioxide films can be produced by active evaporation of
18 silicon monoxide with oxygen assisted deposition (IAD). In addition to
19 the benefits of ion bombardment on film properties, this approach can
20 offer attractive advantages over electron beam evaporation of silicon
21 dioxide. For instance, the evaporation source can be relatively cheap,
22 simple, and easier to control. The production of silicon dioxide films
23 on over 41 inches diameter by resistance evaporation of silicon monoxide

1 and simultaneous oxygen ion bombardment from a cold cathode ion
2 source has also been achieved. Additionally, processes have been
3 developed to convert silicon monoxide to silicon dioxide during deposition
4 by the use of an ion beam. However, additional oxygen should be
5 supplied in a sufficiently energetic process to provide the material
6 conversion during or after the silicon monoxide deposition on the
7 surface.

8 Referring next to Fig. 3, a stack 16 of materials is provided over
9 dielectric layer 14. Stack 16 can comprise, for example, a conductively
10 doped silicon layer 18 (for instance, either n-type doped or p-type doped
11 polysilicon), a metal silicide layer 20 (for instance, titanium silicide or
12 tungsten silicide), and an insulative material layer 22 (for instance, either
13 silicon nitride or SiO_2). Stack 16 can ultimately be utilized for forming
14 a transistor gate. It is noted that the shown stack 16 is an exemplary
15 mass which can be provided over dielectric layer 14. Other masses can
16 be provided over dielectric material 14, and, for example, other
17 conductive layers can be provided over dielectric material 14. In the
18 shown embodiment, a patterned photoresist block 24 is shown formed
19 over stack 16. Photoresist block 24 can be formed by, for example,
20 providing a layer of photoresist over stack 16 and subsequently patterning
21 the layer of photoresist utilizing photolithographic methods. Block 24
22 defines a transistor gate shape therebeneath.

Referring to Fig. 4, a pattern is transferred from photoresist block 24 to stack 16 to form a transistor gate structure 26 comprising the materials of stack 16. Subsequently, source/drain regions 28 and 30 can be formed by implanting conductivity-enhancing dopant through dielectric material 14 and into substrate 12. Stack 16 and source/drain regions 28 and 30 together define a transistor structure. It is noted that patterned stack 16 comprises opposing sidewalls 32 and 34, and that source/drain regions 28 and 30 are shown extending to about opposing sidewalls 32 and 34. In practice, the shown source/drain regions 28 and 30 would typically be lightly-doped diffusion regions. Fig. 5 shows that sidewall spacers 36 and 38 can be formed adjacent opposing sidewalls 32 and 34, respectively, and that heavily-doped source/drain regions 40 and 42 can then be formed within substrate 12 by implanting conductivity enhancing-dopant into the substrate. Sidewall spacers 36 and 38 can comprise, for example, an insulative material such as silicon dioxide or silicon nitride, and can be formed by providing the insulative material along sidewall edges 32 and 34 and subsequently anisotropically etching the insulative material. Source/drain regions 28, 30, 40 and 42 can comprise either n-type and p-type conductivity-enhancing dopant.

Fig. 5 also shows that photoresist block 24 (Fig. 4) is removed from over transistor gate structure 26.

Referring next to Fig. 6, wafer fragment 10 is shown at a processing step that can follow the processing of either Fig. 3 or Fig. 4.

Specifically, the processing step of Fig. 6 shows dielectric material 14 patterned with the stack 16, and accordingly shows dielectric material 14 having sidewall edges co-extensive with sidewall edges 32 and 34 of patterned stack 16. The processing step of Fig. 6 can follow the processing of Fig. 3 if the patterning of stack 16 comprises an etch that extends into dielectric material 14. Alternatively, the structure of Fig. 6 can follow the processing of Fig. 4 if a subsequent etch is utilized after the etching of stack 16 to further etch into dielectric material 14.

Fig. 7 shows wafer fragment 10 at a processing step subsequent to that of Fig. 6, and shows sidewall spacers 36 and 38 formed adjacent opposing sidewalls 32 and 34 analogously to the processing described above with reference to Fig. 5.

After spacers 36 and 38 are formed, a conductivity enhancing dopant can be implanted into substrate 12 to form heavily doped source/drain regions 40 and 42. Transistor gate 26, together with regions 40, 42, 28 and 30, defines a transistor structure. In subsequent processing, one of the source/drain regions can be connected to a capacitor structure 50, and the other connected to a bit line 52 to define a DRAM cell.

Fig. 8 illustrates another embodiment of the present invention, and illustrates how a dielectric material formed in accordance with the present invention can be utilized in a flash memory cell. Specifically, Fig. 8 illustrates a wafer fragment 60 comprising a substrate 62 and a

1 flash memory cell 64 supported by substrate 62. Substrate 62 can
2 comprise monocrystalline silicon, and can be similar or identical to the
3 substrate 12 described above with reference to Figs. 1-7.

4 Memory cell 64 comprises a gate structure 66 and source/drain
5 regions 68 and 70. Memory cell 64 is shown schematically in Fig. 8,
6 and is to be understood that the memory cell can comprise other
7 features, such as, for example, spacers, and additional source/drain
8 regions, including heavily doped and/or lightly doped regions. Gate
9 structure 66 comprises a floating gate 72, and a control gate 74.
10 Gates 72 and 74 comprise conductive materials, such as, for example,
11 conductively doped silicon (for example, conductively doped polysilicon)
12 and/or metals and/or metal silicide. Floating gate 72 is separated from
13 substrate 62 by a dielectric material 76, and gates 74 and 72 are
14 separated from one another by a second dielectric material 78. One or
15 both of dielectric materials 76 and 78 can comprise silicon-doped
16 aluminum oxide, and can be formed by the methodology of the present
17 invention, such as the methodology shown schematically in Fig. 9.. In
18 preferred embodiments, the intergate dielectric material 78 will comprise
19 silicon-doped aluminum oxide, and in particular embodiments can consist
20 of silicon-doped aluminum oxide.

21 It is noted that relative positions are indicated herein and in the
22 claims that follow by elevational terms such as "over." It is to be
23 understood that such elevational terms are defining only relative positions

1 of structural elements to one another, and not absolute elevational
2 positions. Thus, a structure referred to herein as being "over" another
3 can appear to be either under, over or beside the other structure to an
4 external observer viewing a device encompassed by the claims.

5 In compliance with the statute, the invention has been described
6 in language more or less specific as to structural and methodical
7 features. It is to be understood, however, that the invention is not
8 limited to the specific features shown and described, since the means
9 herein disclosed comprise preferred forms of putting the invention into
10 effect. The invention is, therefore, claimed in any of its forms or
11 modifications within the proper scope of the appended claims
12 appropriately interpreted in accordance with the doctrine of equivalents.
13
14
15
16
17
18
19
20
21
22
23